RISC-V ISA Simulator:

Design Documentation

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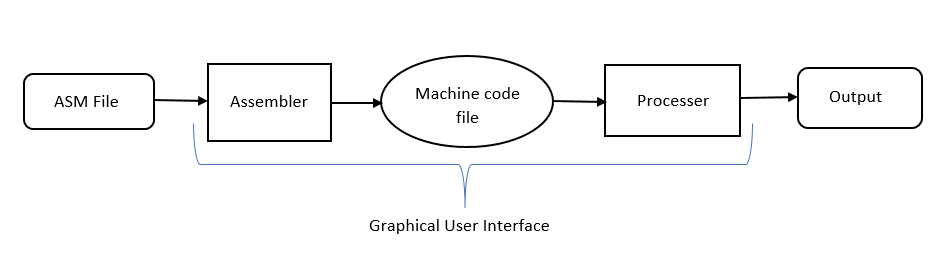
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**Features:**

* **Simulator backend:** Python
* **ISA:** RISC-V RV32IM
* **Size of instruction:** 32 bits
* **Number of registers:** 32
* **Size of registers:** 32 bits

**Overview:**

**Phase 1: Five step instruction execution**

## Input:

Input to the simulator is a machine code file that contains the encoded instruction and the corresponding address at which instruction is supposed to be stored, separated by space.

Functional behaviour:

All the instructions given in the input .mc file is executed as per the functional behaviour of the instructions. Each Instruction will go through the following steps:

* Step 1: **Fetch:** It gets the instruction and increment the PC, and prints that the instruction is fetched and PC is incremented.
* Step 2: **Decode:** Identify the instruction and registers (source and destination), and prints the operation, rs1, rs2, rd.
* Step 3: **Execute:** ALU operations is done or effective address calculation for load, store instructions. The control circuitry select the ALU operation and either Read data from the registers or a sign-extended immediate value as inputs to the ALU, then prints the instruction statement.
* Step 4: **Memory Access:** Read/write data from/to the memory. The control lines set in this stage are Branch, Memory Read, and Memory Write. Then print the retrieved memory at the memory address.
* Step 5: **Register Update or Writeback:** update destination register, and print the result updated in the destination register.

# Test plan:

We test the simulator with following assembly programs:

* Fibonacci Program
* Factorial Program
* Simple addition

**Phase 2: Pipeline implementation with and without data forwarding**

**Input:**

Input is the same that is a machine code file.

**Pipeline Vs Non-Pipeline:**

|  |  |
| --- | --- |
| Pipeline | non pipeline |
| In pipelining system, multiple instructions are overlapped during execution. | In a Non-Pipelining system, processes like decoding, fetching, execution and writing memory are merged into a single unit or a single step. |
| Many instructions are executed at the same time. | Only one instruction is executed at one time. |
| CPI (ideal) is 1 | CPI is 5 |

**Pipeline Hazards:**

**Structural Hazard**

When a planned instruction cannot execute in the proper clock cycle because the hardware does not support the combination of instructions that are set to execute.

**Data Hazards**

Also called a **pipeline data hazard**. When a planned instruction cannot execute in the proper clock cycle because data that are needed to execute the instruction are not yet available.

**Solution:**

**Forwarding**

Also called **bypassing**. A method of resolving a data hazard by retrieving the missing data element from internal buffers rather than waiting for it to arrive from programmer-visible registers or memory.

* We have included forwarding paths from:
* M to M
* M to E
* E to E

**Stalling**

Also called **bubble**. A stall initiated in order to resolve a hazard.

**Control hazard**

Also called **branch hazard**. When the proper instruction cannot execute in the proper pipeline clock cycle because the instruction that was fetched is not the one that is needed; that is, the flow of instruction addresses is not what the pipeline expected.

**Solution:** (We used static branch prediction)

**Branch prediction**

A method of resolving a branch hazard that assumes a given outcome for the conditional branch and proceeds from that assumption rather than waiting to ascertain the actual outcome.

**Branch Target Buffer (BTB):**

* Stores the address of control instructions.
* Stores the target address (if Taken) for each of them.
* Indexed using PC!

The simulator prints messages at the end of simulation:

* Stat1: Total number of cycles
* Stat2: Total instructions executed
* Stat3: CPI
* Stat4: Number of Data-transfer (load and store) instructions executed
* Stat5: Number of ALU instructions executed
* Stat6: Number of Control instructions executed
* Stat7: Number of stalls/bubbles in the pipeline
* Stat8: Number of data hazards
* Stat9: Number of control hazards
* Stat10: Number of branch mispredictions
* Stat11: Number of stalls due to data hazards
* Stat12: Number of stalls due to control hazards